Novel High-Isolation FET Switches

Nobuaki Imai, Akira Minakawa, and Hiroshi Okazaki

Abstract—**This paper describes novel high-isolation monolithic microwave/millimeter-wave integrated circuit (MMIC) field-effect transistor (FET) switches that have higher isolation characteristics than conventional switches without much insertion loss degradation. The newly developed switches consist of series/shount FET's and T-shaped R-C-R circuit. Each FET switch utilizes the parasitic capacitive component of the FET's in the off-state to produce a band-rejection filter at the operating frequency. The design method of the newly proposed switches and their characteristics are described herein. With this method, the isolation characteristics are improved by more than 15 dB between 5.4 GHz and 6.4 GHz and more than 20dB between 5.5 GHz and 6.1 GHz over conventional values.**

I. Introduction

RECENTLY, with the advancement of system functions [1], [2], control devices such as switches have become very important in microwave device applications. Until now, several types of field-effect transistor (FET) switches have been reported [3]–[6], but due to the trade-off between their isolation characteristics and insertion loss they have all had limited performance. Namely, using conventional techniques, achieving high isolation characteristics consistently with low insertion loss has been difficult. This is because when the operating frequency increases, the isolation characteristics deteriorate due to the capacitive component of the FET's in the off-state.

Several papers have focused on resonating the capacitive component at a specified frequency band to obtain high isolation characteristics [7], [8]; [7] is particularly suited for high-powered operation. However, such isolation characteristics (around 40dB) are unsatisfactory for systems requiring extremely accurate characteristics [1], [9]. The above papers involved lumped-element inductances [7] or distributed circuits [8], which put limits on the necessary size reduction to achieve switches capable of operating in the microwave frequency bands.

This paper proposes a new technique that can provide high-isolation FET switches with low insertion loss. Switches newly developed with this method have high-speed switching capabilities because they use fewer FET's than compared with conventional switches to get the same isolation characteristics at the specified frequency band. In addition, the chip size for these switches can be made smaller than the conventional chip size because not only fewer FET's are needed but R-C components are also used. The design method for the newly developed switches is based on making a band-rejection filter using the R-C components at the operating frequency; the construction involves series/shunt FET's and a T-shaped R-C-R circuit. To make the band-rejection filter at the operating frequency, each FET switch utilizes the parasitic capacitive component of the FET's in the off-state.

The design method and the characteristics of the switches are subsequently described. Using this method, the isolation characteristics of the newly developed switches are improved more than 15 dB between 5.4 GHz and 6.4 GHz, and more than 20dB between 5.5 GHz and 6.1 GHz over conventional values. The insertion loss and isolation characteristics of the switch tuned to around 2 GHz are superior to those reported in [3], [6].

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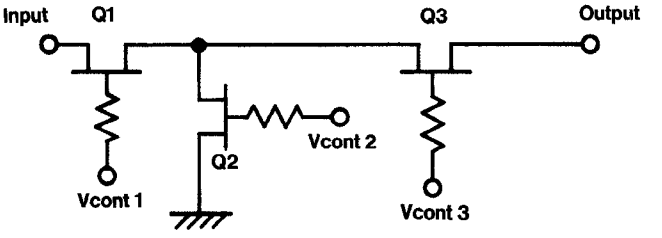


Fig. 1. Circuit configuration of a conventional FET switch.

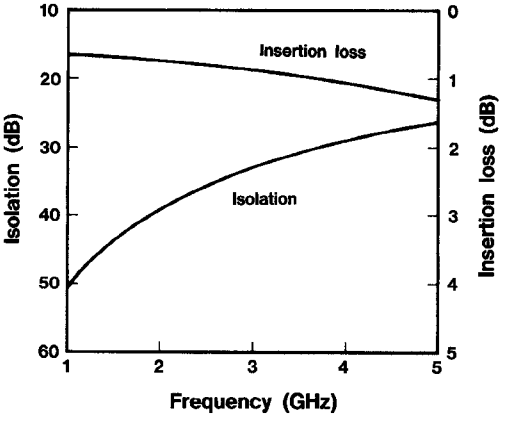


Fig. 2. Simulated frequency response of the conventional FET switch shown in Fig. 1.

II. Principle of the Newly Proposed Switches and Their Design Method

Fig. 1 shows the circuit configuration of a conventional FET switch. In this switch, the parasitic capacitive component of the FET's in the off-state adversely affects the isolation characteristics of the FET's at the high-freqency band. Fig. 2

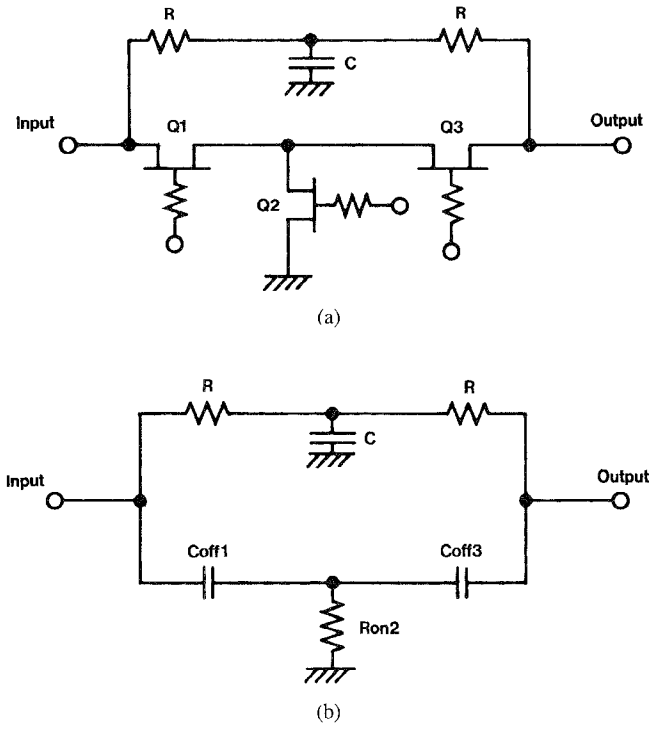


Fig. 3. (a) Circuit configuration of the newly developed FET switch and (b) its equivalent circuit in the off-state

shows the simulated frequency response results of the switch. This figure shows that as the frequency increases, the isolation characteristics deteriorate.

Fig. 3(a) shows the newly developed switch capable of overcoming this problem. A T-shaped R-C-R circuit is added over the conventional FET switch configuration to enable a band-rejection filter to be in the off-state. Fig. 3(b) shows the equivalent circuit of the newly developed FET switch in the off-state. In the "off-state," transistors Q_1 and Q_3 are in their "off-state," but, transistor Q_2 is in its "on-state."

When transistors Q_1 and Q_3 are in their "off-state," they can be equivalently expressed as a parallel circuit of resistance R_{off} and capacitance C_{off}. In the "off-state" of a transistor, R_{off} is much larger than $1/\omega \cdot C_{\text{off}}$. As a result, Q_1 and Q_3 are equivalently expressed as C_{off1} and C_{off3}, respectively. When transistor Q_2 is in its "on-state," it can be equivalently expressed as a series resistance R_{on2}. Considering these points, the newly developed FET switch shown in Fig. 3(a), when it is in the "off-state," can be equivalently expressed by the circuit shown in Fig. 3(b). This circuit is referred to as the twin-T circuit [10], and its transfer function can be expressed as follows [11]

$$T(s) = \frac{as^3 + bs^2 + cs + 1}{as^3 + (b+d)s^2 + (c+e)s + 1} \tag{1}$$

where

$$a = R^2 R_{\text{on2}} C C_{\text{off1}} C_{\text{off3}}, b = 2RR_{\text{on2}} C_{\text{off1}} C_{\text{off3}},$$
$$c = R_{\text{on2}}(C_{\text{off1}} + C_{\text{off3}})$$
$$d = RC\{RC_{\text{off3}} + R_{\text{on2}}(C_{\text{off1}} + C_{\text{off3}})\},$$
$$e = RC + 2RC_{\text{off3}}.$$

It is obvious that this transfer function is a 3rd-order function. However, when the following conditions are satisfied, the transfer function of the twin-T circuit degenerates into a 2nd-order function [12]

$$RC = 2R_{\text{on2}} \cdot (C_{\text{off1}} + C_{\text{off3}}). \tag{2}$$

When this condition is satisfied, the transfer function $T(s)$ can be expressed as follows:

$$T(s) = \frac{2s^2 C_{\text{off1}} C_{\text{off3}} R_{\text{on2}} R + 1}{2s^2 C_{\text{off1}} C_{\text{off3}} R_{\text{on2}} R + sR(2C_{\text{off3}} + C) + 1}. \tag{3}$$

This means that by selecting the values for the RC components which satisfy (2), the twin-T circuit shown in Fig. 3(b) becomes a band-rejection filter. The center frequency of the band-rejection filter determined from (3) can be expressed as follows:

$$f_0 = \frac{1}{2\pi\sqrt{2C_{\text{off1}} C_{\text{off3}} R_{\text{on2}} R}}. \tag{4}$$

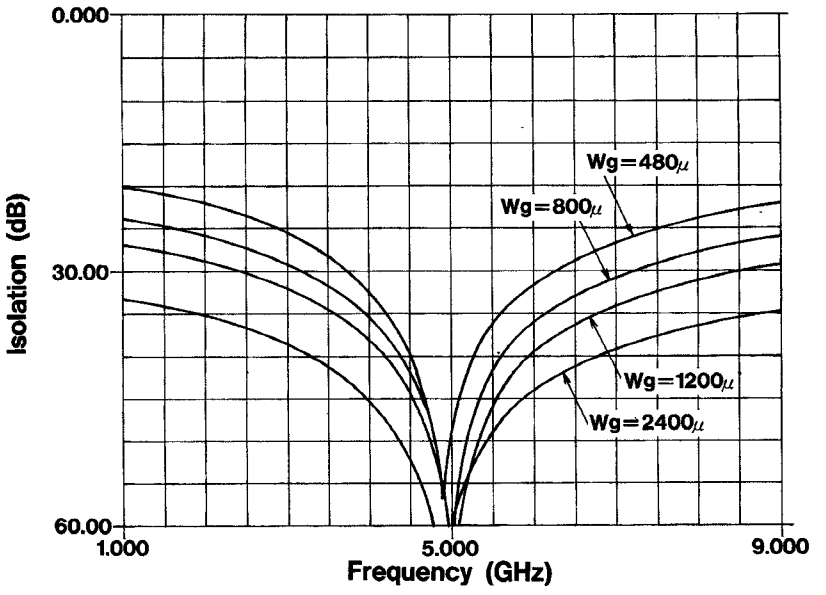
When the parameters $C_{\text{off1}}, R_{\text{on2}}, C_{\text{off3}}$ of transistors Q_1, Q_2, Q_3 are known, the value of R can be determined from (4) according to the operating frequency band of the switch. Consequently, the value of C can be determined from (2). The above analysis assumes that the network feeds into an infinitely high-load impedance. However, the switch shown in Fig. 3 feeds into a load impedance Z_L of 50 ohms. As a result, the condition in (2) should be modified slightly (see Appendix). The optimum value of C is determined using "Libra" to get the maximum rejection at the operating frequency band.

III. Parameter Dependence in the Characteristics of the Switches

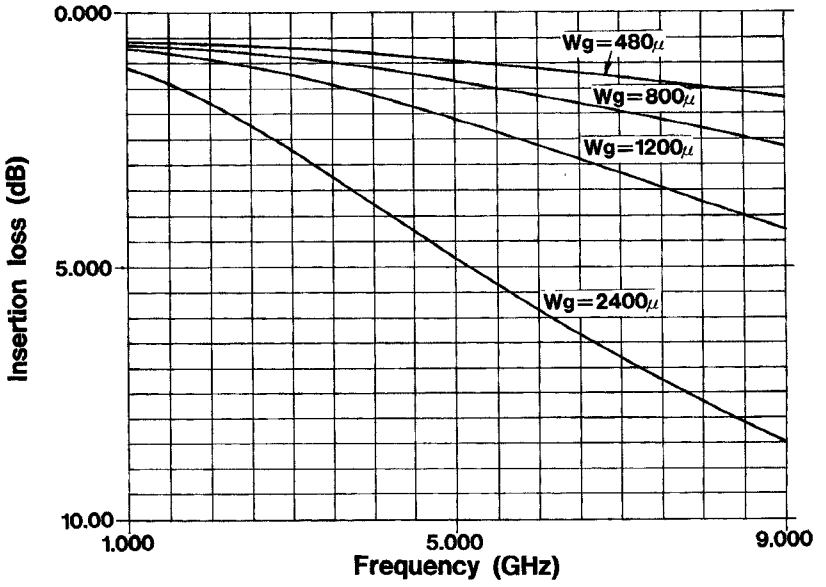
Fig. 4 shows simulated frequency responses for different sizes of transistor Q_2. Fig. 4(a) illustrates isolation characteristics for different sizes of transistor Q_2 at the optimum capacitance value. Fig. 4(b) gives insertion loss characteristics calculated under the same condition. In the calculations of Fig. 4, transistors Q_1 and Q_3 were assumed to have a fixed size of 800 μm. The center frequency of the switches was set to 5.0 GHz.

Equation (4) predicts that when the FET parameters are known, the operating frequency of the switches can be determined by the value of R. The optimum isolation characteristics at the specified frequency band can be obtained by choosing the value of C. These R and C values are shown in the table of Fig. 4 for different sizes of transistor Q_2. They can be set within an accuracy of $\pm 10\%$ when fabricated with MMIC's. When R and C deviate from their assigned values due to errors in the process, the calculated deviation of the center frequency and the maximum isolation are less than $\pm 5.5\%$ and 2 dB, respectively. However, the deviation is within permitted limits.

Fig. 5 shows simulated frequency responses obtained when the sizes of transistors Q_1 and Q_3 were changed. Fig. 5(a) gives isolation characteristics and Fig. 5(b) gives insertion loss



(a)



(b)

Wg=480μ	R=400Ω, C=0.04pF	Wg=1200μ	R=95Ω, C=0.01pF
Wg=800μ	R=65Ω, C=0.014pF	Wg=2400μ	R=20Ω, C=0.005pF

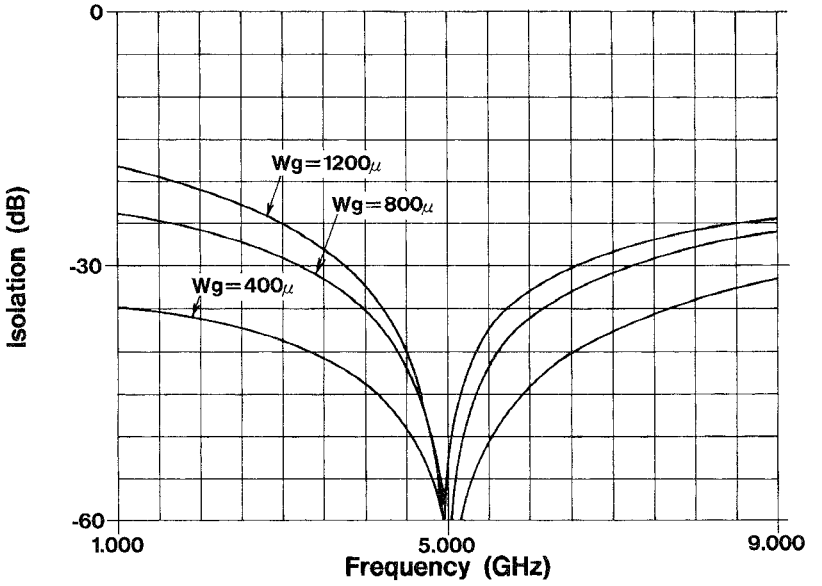
(c)

Fig. 4. Simulated frequency responses when the size of transistor Q_2 is changed. (a) Isolation characteristics when the size of transistor Q_2 is changed. (b) Insertion loss characteristics when the size of transistor Q_2 is changed. (c) R and C values for different sizes of transistor Q_2.

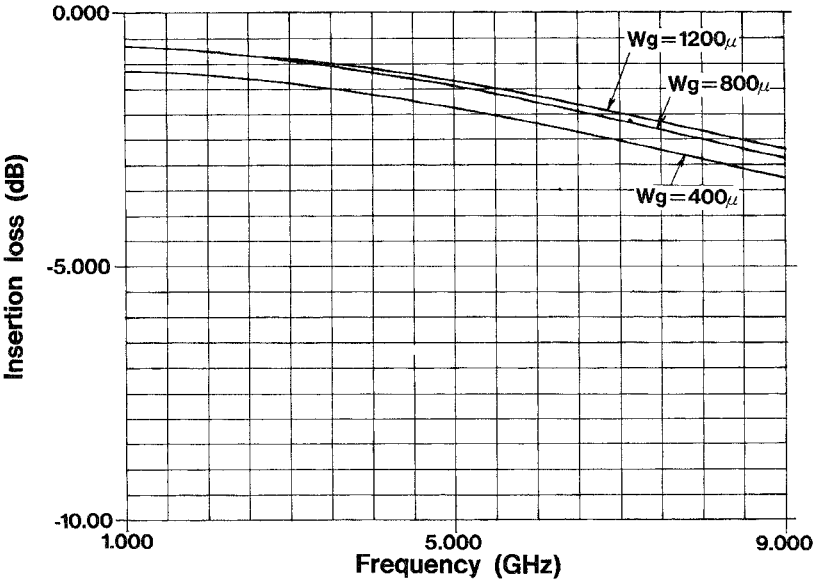
characteristics. In the calculations of Fig. 5, the value of R was selected to get the center frequency of 5 GHz, and the value of C was selected to get the maximum isolation at 5.0 GHz as in Fig. 4. These R and C values are shown in the table of Fig. 5 for different sizes of transistors Q_1 and Q_3.

From Fig. 4, it can be seen that a larger FET Q_2 size leads to higher isolation characteristics. When the size of FET Q_2 is too large, however, the internal capacitance of Q_2 when it is in the "off" state increases. Accordingly, the insertion loss of the switch increases especially at higher frequency bands. As a result, there is a trade-off between the isolation characteristics and the insertion loss characteristics.

This tendency is also found in Fig. 5. When the sizes of FET Q_1 and FET Q_3 are small, in other words, when the capacitive component of Q_1 and Q_3 in the "off" state are small, higher isolation characteristics are obtained. In this case, the on-



(a)



(b)

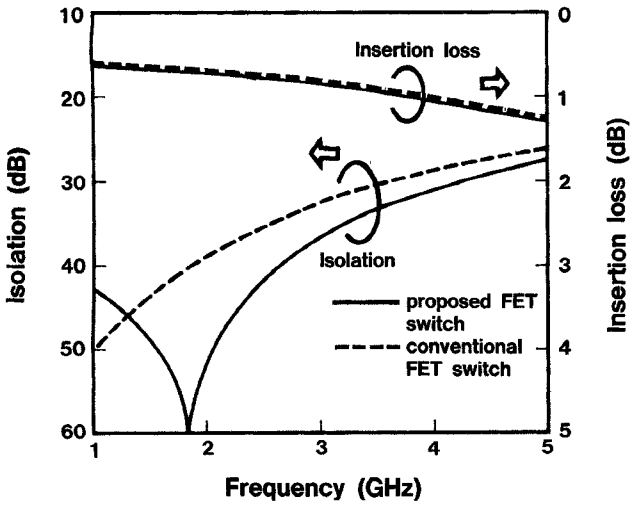
Wg=400μ	R=4000Ω, C=0.004pF
Wg=800μ	R=2000Ω, C=0.014pF
Wg=1200μ	R=1333Ω, C=0.04pF

(c)

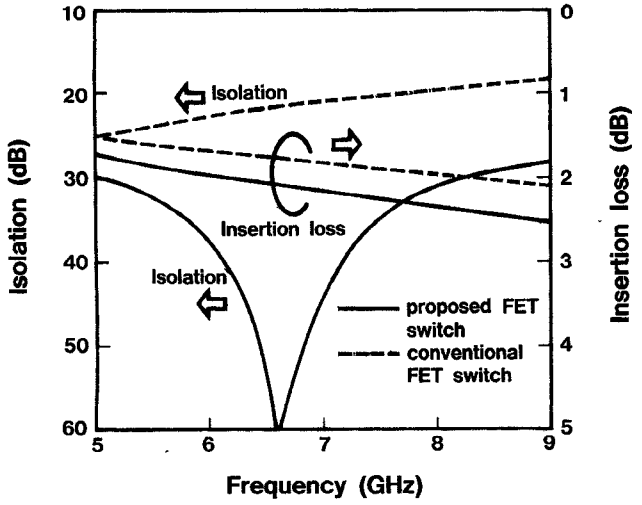
Fig. 5. Simulated frequency responses when the size of transistors Q_1 and Q_3 are changed. (a) Isolation characteristics when the size of transistors Q_1 and Q_3 are changed. (b) Insertion loss characteristics when the size of transistors Q_1 and Q_3 are changed. (c) R and C values for different sizes of transistors Q_1 and Q_3.

resistances (R_{on}) of Q_1 and Q_3 become large, leading to a larger insertion loss of the switch. This trend is additionally found in the conventional switch shown in Fig. 1.

These simulated results provide design information about the insertion loss and isolation characteristics. Figs. 4(b) and 5(b) show that, to get insertion loss characteristics of less than 1.5 dB at 5.0 GHz, the gate widths of Q_1 and Q_3 should be larger than 800 μm, and that of Q_2 should be smaller than 800 μm. Figs. 4(a) and 5(a) show that, to get isolation characteristics of more than 40 dB over 20% of the bandwidth around the center frequency, the gate widths of Q_1 and Q_3 should be smaller than 800 μm, and that of FET Q_2 should be larger than 800 μm. Considering these points, in the following experiment, all FET's were set with a gate width of 800 μm.

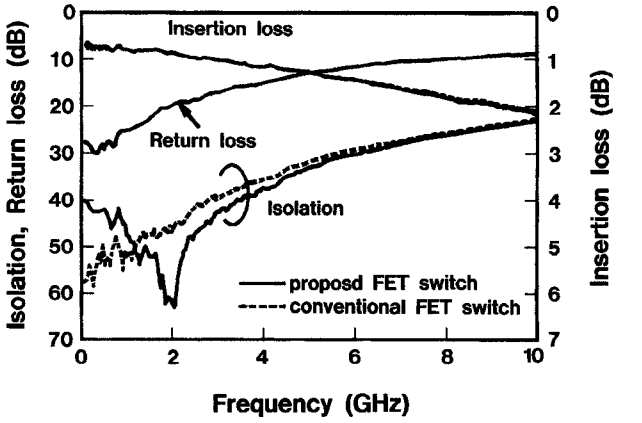


(a)

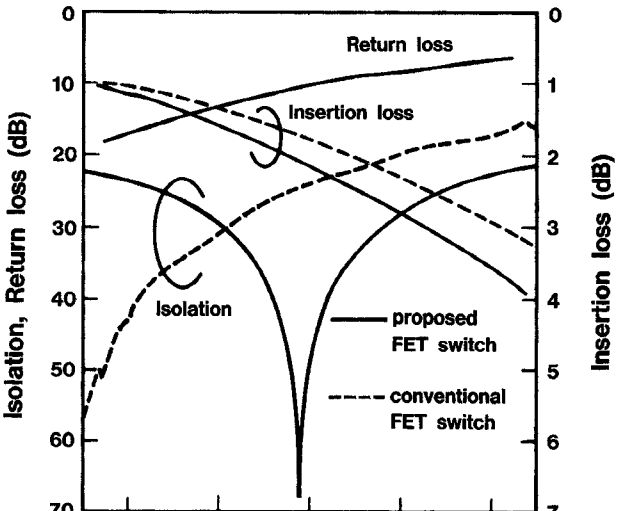


(b)

Fig. 6. Simulation results for the proposed FET switch and a conventional series/shunt switch. (a) Tuned to 2 GHz-band. (b) Tuned to 6 GHz-band.



(a)



(b)

Fig. 7. Experimental frequency response of the switch. (a) Tuned to 2 GHz-band. (b) Tuned to 6 GHz-band.

Fig. 6 compares simulated frequency response results obtained from the newly developed switch and those of a conventional switch, both with FET's of the same sizes. This figure shows that the isolation characteristics are improved with the new switch at the specified frequency bands.

Sensitivity of the design methodology to variations in the process parameters is also examined. When the capacitive components of transistors Q_1 and Q_3 in the off-state deviate from their design values by 10%, the calculated deviation of the center frequency is less than 10%. In contrast, when on resistance R_{on2} of transistor Q_2 deviates from its design value by 10%, the calculated deviation of the center frequency is less than 5%. In both cases, the impedance of the transistors is extracted from the impedance measurement.

IV. Experimental Results

The FET's used in the experiments were SAINT [13] or pulse-doped GaAs FET's [14] with a gate width of $Wg = 800\,\mu$m. Fig. 7 shows the experimental frequency response of the newly developed switch and a conventional switch. As was expected from the theoretical considerations described above, the isolation characteristics of the newly developed switch could be improved. Fig. 7(a) and (b), show results obtained at the 2 GHz, and 6 GHz bands, respectively. For example, around the 6 GHz band the isolation characteristics are improved by more than 15 dB between 5.4 GHz and 6.4 GHz, and more than 20dB between 5.5 GHz and 6.1 GHz. The increase in insertion loss for the newly developed switch over the conventional switch is less than 0.3 dB at the 6 GHz band. Therefore, the newly developed switch has improved isolation characteristics over the conventional one with small insertion loss degradation. (If isolation characteristics of more than 50 dB at 6GHz are to be obtained using the conventional method, the insertion loss will increase by about 2 dB because the switches need to be cascaded.) It would seem that the deviation of the center frequency found in the experiment from

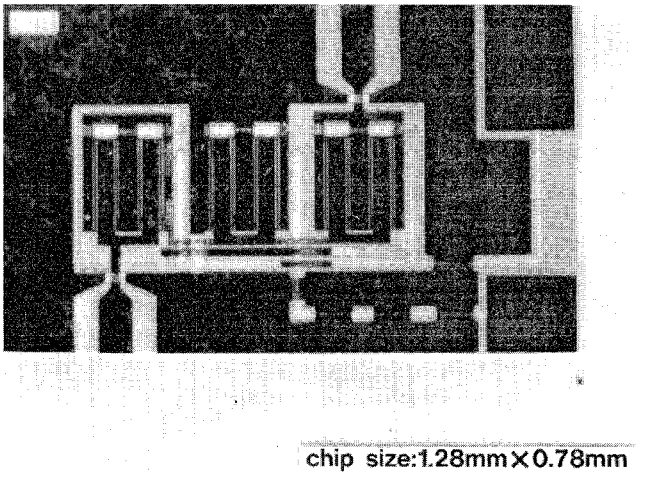


Fig. 8. Photograph of the proposed FET switch.

that of the simulated results (Fig. 6) is due to the difference in transistor parameters.

The input–output characteristics of the switch were measured. At the input level of 10 dBm, an IM3 of less than 50dBc was obtained. The transient response characteristics of the newly developed switch was also measured. The rise time and fall time were less than 1.0 nsec at the operating frequency of 6 GHz. The newly developed switch uses fewer FET's compared to the conventional switch to get the same isolation at the specified frequency band, leading to a high-speed switching operation. (The switching speed in [15] is 2.0 nsec at 1.0 GHz with isolation characteristics of more than 27 dB.)

Fig. 8 shows a photograph of the fabricated MMIC FET switch. Because only RC components are added over the conventional switch circuit, the entire chip size is only 1.28 mm × 0.78 mm.

V. Conclusion

Novel high-isolation MMIC FET switches have been proposed that have higher isolation characteristics than conventional switches without much insertion loss degradation. The newly developed switches consist of series/shunt FET's and a T-shaped R-C-R circuit. The FET switch utilizes the parasitic capacitive component of the FET's in the off-state to produce a band-rejection filter at the operating frequency. The design method of this newly developed switch was described and it was confirmed that the predicted calculated results agreed well with the experimental results. The distortion characteristics and switching speed were also examined experimentally. These MMIC FET switches will help to produce multifunctional MMIC circuits.

Appendix

The F-matrix of T-type circuits composed of R-C-R and C-R-C components, as shown in Fig. 3(b) can be expressed as follows:

$$(F)_1 = \begin{pmatrix} A_1 & B_1 \\ C_1 & D_1 \end{pmatrix} \tag{A1}$$

$$(F)_2 = \begin{pmatrix} A_2 & B_2 \\ C_2 & D_2 \end{pmatrix} \tag{A2}$$

$$\begin{aligned} A_1 &= 1 + sCR \\ B_1 &= 2R + sC \cdot R^2 \\ C_1 &= sC \\ D_1 &= 1 + sCR \\ A_2 &= 1 + \frac{1}{sC_{\text{off1}}R_{\text{on2}}} \\ B_2 &= \frac{1}{sC_{\text{off1}}} + \frac{1}{sC_{\text{off2}}} + \frac{1}{s^2C_{\text{off1}}C_{\text{off3}}R_{\text{on2}}} \\ C_2 &= \frac{1}{R_{\text{on2}}} \\ D_2 &= 1 + \frac{1}{sC_{\text{off3}}R_{\text{on2}}}. \end{aligned}$$

When these T-type circuits are connected in parallel to form a twin-T circuit, the resulting F matrix can be expressed as follows:

$$\begin{aligned} (F)_t &= \frac{1}{B_1 + B_2}\begin{bmatrix} A_1B_2 + B_1A_2 & B_1B_2 \\ -\begin{vmatrix} A_1 - A_2 & B_1 + B_2 \\ C_1 + C_2 & D_1 - D_2 \end{vmatrix} & D_1B_2 + B_1D_2 \end{bmatrix} \\ &= \begin{bmatrix} A_t & B_t \\ C_t & D_t \end{bmatrix}. \end{aligned} \tag{A3}$$

The transfer function of the twin-T circuit shown in Fig. 3(b) can be expressed as follows:

$$\begin{aligned} A_v &= V_2/V_1 = (A_t + B_t/R_L)^{-1} \\ &= \left(\frac{A_1B_2 + B_1A_2}{B_1 + B_2} + \frac{B_1B_2}{R_L(B_1 + B_2)}\right)^{-1} \end{aligned} \tag{A4}$$

where R_L is the load resistance.

When (A1) and (A2) are substituted into (A4), A_v can be expressed as follows:

$$A_v = \frac{as^3 + bs^2 + cs + 1}{(as^3 + bs^2 + cs + 1) + (ds^2 + es + f)} \tag{A5}$$

where

$$\begin{aligned} a &= \alpha CR^2 = CR^2R_{\text{on2}} \cdot C_{\text{off1}} \cdot C_{\text{off3}} \\ b &= 2\alpha R = 2RR_{\text{on2}} \cdot C_{\text{off1}} \cdot C_{\text{off3}} \\ c &= \frac{\alpha}{Ct} = R_{\text{on2}}(C_{\text{off1}} + C_{\text{off3}}) \\ d &= \frac{\alpha CR^2}{R_LCt} + \alpha\left(\frac{CR}{Ct} + \frac{CR^2}{C_{\text{off1}} \cdot R_{\text{on2}}}\right) \\ e &= \frac{\alpha}{Ct}(\gamma Ct - 1) + \frac{CtCR^2 + 2R\alpha}{R_LCt} \\ f &= \frac{2R}{R_L} \\ \alpha &= C_{\text{off1}} \cdot C_{\text{off3}} \cdot R_{\text{on2}} \\ \gamma &= \frac{1}{Ct} + \frac{CR}{\alpha} + \frac{2R}{C_{\text{off1}} \cdot R_{\text{on2}}} \\ 1/Ct &= \frac{1}{C_{\text{off1}}} + \frac{1}{C_{\text{off3}}}. \end{aligned}$$

When load resistance R_L reaches infinity, f becomes zero,

and d and e are transformed as follows:

$$d = \alpha\left(\frac{CR}{Ct} + \frac{CR^2}{C_{\text{off1}} \cdot R_{\text{on2}}}\right)$$
$$= RC\{RC_{\text{off3}} + R_{\text{on2}}(C_{\text{off1}} + C_{\text{off3}})\}$$
$$e = \frac{\alpha}{C_1}(\gamma C_t - 1)$$
$$= RC + 2RC_{\text{off3}}.$$

Accordingly, (A5) becomes (1) when load resistance RL equals infinity. The transfer function expressed in (A5) should degenerate into a 2nd-order function as determined by $as^3 + bs^2 + cs + 1$ and $ds^2 + es + f$ where the two expressions should have a common factor. If they have a common factor, the following condition should be satisfied

$$du^2 + eu + f = 0 \tag{A6}$$

where

$$u = \frac{Kf - d^2}{Ld - Ke}$$
$$K = bd - ae$$
$$L = cd - af.$$

The value of capacitance C in Fig. 3 is determined from these conditions.

If we define A_v as

$$A_v = \frac{s^2 + ks + l}{s^2 + ms + n} \tag{A7}$$

after dividing the numerator and denominator of (A5) by the common factor, the center frequency of the twin-T circuit is determined from the condition that the numerator of (A7) should be zero under the conditions stated in (A6).

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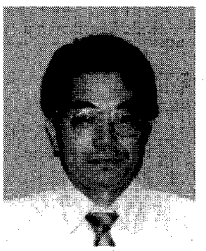
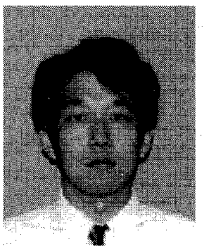


Nobuaki Imai was born in Kochi, Japan in 1953. He received the B.S. degree in electrical engineering from the Nagoya Institute of Technology, Nagoya, Japan in 1975, and the M.S. degree from Kyoto University, Kyoto, Japan, in 1977.

He joined Yokosuka Electrical Communication Laboratories, Japan in 1977, where he was engaged in research on microwave and millimeter wave integrated circuits and the development of digital microwave systems. In 1993, he moved to ATR, where he has been engaged in the research of millimeter wave personal communication systems using optical fiber.

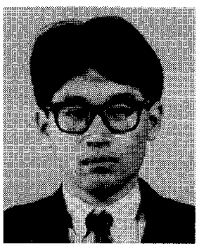
Mr. Imai is a member of the Institute of Electronics Information and Communication Engineers (IEICE) of Japan.



Akira Minakawa was born in Ibaraki, Japan on May 20, 1960. He received B.S. and M.S. degrees in electrical engineering from Ibaraki University, Ibaraki, in 1984 and 1986, respectively.

He joined the Electrical Communications Laboratories of Nippon Telegraph and Telephone Corporation, Yokosuka, Japan, in 1986, where he was engaged in research and development of monolithic microwave integrated circuits. In 1993, he joined ATR Optical and Radio Communications Research Laboratories, where he has worked on research in millimeter-wave integrated circuits for personal communication systems.

Mr. Minakawa is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.



Hiroshi Okazaki was born in Okayama, Japan in 1965. He received the B.E. and M.E. degrees from Osaka University, Osaka, Japan, in 1988 and 1990, respectively.

In 1990, he joined NTT Radio Communication Systems Laboratories, Yokosuka, Japan, and since then he has been involved in the investigation of low power-consumption SSPA's for earth stations. He is currently a Research Engineer at NTT Wireless Systems Laboratories, Yokosuka, Japan, where he is engaged in research on GaAs MMIC design.

Mr. Okazaki is a member of the Institute of Electronics, Information and Communication Engineers (IEICE) of Japan.